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ABSTRACT OF THE DISCLOSURE

There is provided a reset circuit for reducing current consumption during resetting. A reset circuit 20 is constituted in such a manner that a pulse generation circuit 22 for generating a reset pulse signal (PRSTN) 50 from a reset signal input to an input terminal (RSTN) is connected to a plurality modules 10, 12, 14, a register 40 arranged in the module 10 is initialized based on the reset pulse signal (PRSTN) 50, a register 42 arranged in the module 12 of a next stage is initialized based on a module reset signal (MRSTN) 60 output from a control circuit 30 arranged in the module 10 of a previous stage, and a register 44 arranged in each of modules of stages thereafter, e.g., the module 14, is initialized based on a module reset signal (MRSTN) output from a control circuit 32 arranged in the module 12 of a previous stage.